AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An electrical bistable device comprising:

an electrically conductive mixed layer comprising a first side and a second side, said mixed layer comprising a low conductivity material and a high conductivity material wherein said mixed layer is electrically conductive;

a first layer of low conductivity material located on said first side of said mixed layer, said first layer of low conductivity material having a first electrode side;

a second layer of low conductivity material located on said second side of said mixed layer, said second layer of low conductivity material having a second electrode side;

a first electrode attached to said first layer of low conductivity material at said first electrode side;

a second electrode attached to said second layer of low conductivity material at said second electrode side;

a first interface located on the first side of said mixed layer where said first layer of low conductivity material and said mixed layer meet, said first interface being electrically convertible between a stable low resistance state and a stable high resistance state by application of an electrical voltage between the said first electrode and said mixed layer; ~~and~~

a second interface located on the second side of said mixed layer where said second layer of low conductivity material and said mixed layer meet, said second interface being electrically convertible between a stable low resistance state and a stable high resistance state by application of an electrical voltage between the said second electrode and said mixed layer;

a first terminal in electrical connection with said first electrode;

a second terminal in electrical connection with said second electrode; and

a third terminal in electrical connection with said electrically conductive mixed layer.

wherein said stable low resistance states and said stable high resistance states persist free from an applied voltage to provide electrical bistability.

2. (Original) An electrical bistable device according to claim 1 wherein said low conductivity material is selected from the group consisting of organic semiconductors and organic insulators.

3. (Original) An electrical bistable device according to claim 1 wherein said high conductivity material is selected from the group consisting of metals, metal oxides, conducting polymers and organic conductors.

4. (Original) An electrical bistable device according to claim 1 wherein said electrically conductive mixed layer is formed by condensing vapors comprising said high conductivity material and said low conductivity material together to form said electrically conductive mixed layer.

5. (Currently Amended) A method for making a bistable device comprising:

providing a bottom electrode;

forming a layer of low conductivity organic material on said bottom electrode;

forming an electrically conductive mixed layer on said layer of low conductivity material, said electrically conductive mixed layer comprising a low conductivity material and a high conductivity material wherein said mixed layer is electrically conductive and wherein an electrically bistable interface is formed between said layer of low conductivity material and said electrically conductive mixed layer;

forming a second layer of low conductivity material on said electrically conductive layer wherein a second electrically bistable interface is formed between said electrically conductive layer and said second layer of low conductivity material; ~~and~~

forming a top electrode on said second layer of low conductivity material;

electrically connecting a first terminal to said first electrode;

electrically connecting a second terminal to said second electrode; and

electrically connecting a third terminal to said electrically conductive mixed layer.

6. (Original) A method for making an electrical bistable device according to claim 5 wherein said low conductivity material is selected from the group consisting of organic semiconductors and organic insulators.

7. (Original) A method for making an electrical bistable device according to claim 5 wherein said high conductivity material is selected from the group consisting of metals, metal oxides, conducting polymers and organic conductors.

8. (Original) A method for making an electrical bistable device according to claim 5 wherein said electrically conductive mixed layer is formed by condensing vapors of said high conductivity material and said low conductivity material together to form said electrically conductive mixed layer.

9. (Previously Presented) A method comprising the step of applying an electrical voltage between the first and second electrodes of the bistable device according to claim 1 to convert both said first interface and said second interface between said high resistance state and said low resistance state.

10. (Previously Presented) A method comprising the step of applying an electrical voltage between the first electrode and the electrically conductive mixed layer of said electrical bistable device according to claim 1 to convert said first interface between said high resistance state and said low resistance state.

11. (Previously Presented) A method comprising the step of applying an electrical voltage between the second electrode and the electrically conductive mixed layer of said electrical bistable device according to claim 1 to convert said second interface between said high resistance state and said low resistance state.

12. (Currently Amended) A memory device comprising:

an electrically conductive mixed layer comprising a first side and a second side, said mixed layer comprising ~~an~~ a low conductivity material and a high conductivity material wherein said mixed layer is electrically conductive;

a first layer of low conductivity material located on said first side of said mixed layer, said first layer of low conductivity material having a first electrode side;

a second layer of low conductivity material located on said second side of said mixed layer, said second layer of low conductivity material having a second electrode side;

a first interface located on the first side of said mixed layer where said first layer of low conductivity material and said mixed layer meet, said first interface being electrically convertible between a stable low resistance state and a stable high resistance state by application of an electrical voltage to said first interface, a second interface located on the second side of said mixed layer where said second layer of low conductivity material and said mixed layer meet, said second interface being electrically convertible between a stable low resistance state and a stable high resistance state by application of an electrical voltage to said second interface;

a first electrode attached to said first layer of low conductivity material at said first electrode side;

a second electrode attached to said second layer of low conductivity material at said second electrode side;

a memory input element in electrical connection to said first electrode, said second electrode and said electrically conductive mixed layer, said memory input element being constructed to selectively ~~for applying a voltage to said first electrode, said second electrode and/or said electrically conductive mixed layer to~~ convert said first interface and/or said second ~~interfaces~~ interface between said stable low electrical resistance state and said stable high electrical resistance state; and

a memory readout element in electrical connection with said electrically conductive mixed layer which provides an indication of whether said first interface and/or said second interface is in said stable low electrical resistance state or said stable high electrical resistance state,

wherein said stable low resistance states and said stable high resistance states persist free from an applied voltage to provide electrical bistability.

13. (Original) A memory device according to claim 12 wherein said low conductivity material is selected from the group consisting of organic semiconductors and organic insulators.

14. (Original) A memory device according to claim 12 wherein said high conductivity material is selected from the group consisting of metals, metal oxides, conducting polymers and organic conductors.

15. (Original) A memory device according to claim 12 wherein said electrically conductive mixed layer is formed by condensing vapors of said high conductivity and low conductivity materials together to form said electrically conductive mixed layer.

16. (Original) A method for operating a memory device according to claim 12 comprising the step of applying a sufficient electrical voltage to said memory input element to convert said first interface and/or said second interface between said high resistance state and said low resistance state.

17. (Previously Presented) An electrical bistable device according to claim 1, wherein said electrically conductive mixed layer is a two-phase system consisting essentially of electrically conductive nanoparticles dispersed in said low conductivity material.

18. (Previously Presented) An electrical bistable device according to claim 17, wherein said electrically conductive nanoparticles have an average particle size of at least 1nm and less than 50 nm.

19. (Previously Presented) A method for making an electrical bistable device according to claim 8, wherein said condensing forms a two-phase system consisting essentially of electrically conductive nanoparticles dispersed in said low conductivity material.

20. (Previously Presented) A method for an electrical bistable device according to claim 19, wherein said electrically conductive nanoparticles have an average particle size of at least 1 nm and less than 50 nm.

21. (Previously Presented) A memory device according to claim 12, wherein, said electrically conductive mixed layer is a two-phase system consisting essentially of electrically conductive nanoparticles dispersed in said low conductivity material.

22. (Previously Presented) A memory device according to claim 21, wherein said electrically conductive nanoparticles have an average particle size of at least 1nm and less than 50 nm.

23. (New) A memory device according to claim 12, wherein said memory readout element provides said indication of whether said first interface and/or said second interface is in said low electrical resistance state or said high electrical resistance state based on a voltage measurement.